REMARKS

This Amendment is submitted in response to the Examiner's Action mailed November 3, 2004, with a shortened statutory period of three months set to expire February 3, 2005. Claims 1-45 are currently pending. With this amendment, claims 1, 3, 13, 16, 19, 21, 31, 34, 39, 44, and 45 have been amended.

The Examiner objected to the Abstract stating that the title of the invention appears above the abstract and should be deleted. The abstract has been amended to delete the title. Therefore, Applicant believes this objection should be withdrawn.

The Examiner objected to Figure 5, stating that the label for reference numbers 508 and 510 should say "VALUE" instead of "VALVE". This correction has been made. Therefore, Applicant believes this objection should be withdrawn.

The Examiner objected to claims 3 and 21 because of informalities. These claims have been amended to correct the typographical errors. Therefore, Applicant believes this objection should be withdrawn.

The Examiner rejected claims 1, 4-8, 10, 12, 13, 16-19, 22-26, 28, 30, 31, 34, 35, 39, 40, 44, and 45 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,526,433 issued to *Chang* in view of U.S. Patent 5,777,988 issued to *Cisneros*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claims 1, 19, 34, and 44 have been amended to describe each path in the set of paths including a different plurality of a plurality of nodes through which data passes when the data is transmitted via the path. Each path is a different path from the data processing system to the destination. See Applicant's Figure 4. Each one of the nodes stores the same time out value. These claims were also amended to describe the measured latency being a latency through a first plurality of nodes that are included in the identified path. The same time out value is set in each one of the nodes in each one of the paths. For one example of support for these amendments please see Applicant's specification page 10, lines 18-32.

Claims 13, 31, 39, and 45 were amended to describe each path in the plurality of paths including a different plurality of a plurality of nodes through which data passes when the data is transmitted via the path. Each path is a different path to the destination.

See Applicant's Figure 4. Each one of the nodes stores the same time out value. The claims have also been amended to describe the time being a time it takes the data to traverse through a first plurality of nodes that are included in the particular path. The same time out value is set in each one of the nodes in each one of the paths. For one example of support for these amendments please see Applicant's specification page 10, lines 18-32.

Claim 16 was amended to describe each path in the plurality of paths including a different plurality of a plurality of nodes through which data passes when the data is transmitted via the path. Each path is a different path to the destination. See Applicant's Figure 4. Each one of the nodes stores the same time out value. The measured latency is a latency through a first plurality of nodes that are included in the identified path. The same time out value is set in each one of the nodes in each one of the paths. For one example of support for these amendments please see Applicant's specification page 10, lines 18-32.

The Examiner states that *Chang* teaches all of the features of Applicant's claims except for the feature of identifying a path from a set of paths where the identified path has the largest latency of the set of paths. The Examiner uses *Cisneros* to supply the features missing from *Chang* and states that *Cisneros* teaches identifying a path with the maximum latency.

Chang is concerned with the communications between only a pair of computers, i.e. the client/server pair. "Fig. 3 shows that the client/server pair comprising an application client 10A and an application server 10B communicate to each other through remote procedure calls ("RPCs") 106 and 108." Column 5, lines 14-17.

The combination of *Chang* and *Cisneros* does not render Applicant's claims unpatentable, however, because the combination does not teach identifying a path including a different plurality of a plurality of nodes where the same time out value is stored in each node in all of the paths and not just in the identified path.

Chang does not teach a path including a plurality of nodes. *Chang* describes measuring a communication time between each client and server pair. *Chang* does not describe this pair as being a path that includes a plurality of nodes. *Chang* merely teaches a server being connected to a client. *Chang* does not teach a path including a

different plurality of a plurality of nodes through which data passes when the data is transmitted via the path.

Chang does not teach storing a time out value in each node in a path. *Chang* teaches a time out value for a client and server pair being set for each pair of client and servers. *Chang* teaches that this time out value is stored in the client. See column 5, lines 43-48.

Chang does not teach storing the same time out value in each node. Since the time out value is determined for a particular client/server combination, the time out values for each combination are very likely different from one another. Each client stored the time out value determined for its own client/server pair. Therefore, the time out values stored by each client will be different. Further, *Chang* does not teach that the time out values stored in each client are the same time out values.

Chang does not describe identifying a path from a set of different paths, using that path to determine the latency, and then setting the time out value using this latency. *Cisneros* teaches paths that include multiple nodes where a time through the paths differs. *Cisneros* does not describe, however, identifying a path, using that path to determine the latency, and then setting the time out value using this latency. The combination of the two references does not describe identifying a path, using that path to determine the latency, and then setting the time out value using this latency.

Applicant claims each path including a different plurality of a plurality of nodes. The time out value is then set in the plurality of nodes. These are the nodes in the plurality of paths, and not just in the identified or particular path. The combination of references does not describe setting the time out value in the plurality of nodes in paths other than the identified path.

The combination of references does not describe, teach, or suggest Applicant's claims. Therefore, Applicant's claims are believed to be patentable over the prior art.

The Examiner rejected claims 36-38 and 41-43 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,526,433 issued to *Chang* in view of *Cisneros* and further in view of "The RS/6000 Enterprise Server Model S80 Technology and Architecture Technical White Paper" [hereinafter *Technical White Paper*]. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

The Examiner stated that neither *Chang* nor *Cisnerso* teaches a data processing system that includes a bus including a primary bus and secondary bus, and where the I/O controller is a modem or Ethernet adapter. The Examiner used *Technical White Paper* to add the features believed missing from the combination of *Chang* and *Cisnerso*.

The combination of references does not teach a path including a different plurality of a plurality of nodes where a time out value is stored in each node in all of the paths and not just in the identified path in combination with the bus including a primary bus and secondary bus and where the I/O controller is a modem or Ethernet adapter. Therefore, the combination does not render Applicant's claims unpatentable.

The Examiner rejected claims 2, 3, 11, 14, 15, 20, 21, 29, 32, and 33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,526,433 issued to *Chang* in view of *Cisneros* and further in view of U.S. Published Patent Application 2004/0037233 published by *Suzuki*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

The Examiner stated that neither *Chang* nor *Cisnerso* teaches setting a time out value by adding a period of time or percentage of the measured latency to the time out value. The Examiner used *Suzuki* to add the features believed missing from the combination of *Chang* and *Cisnerso*.

The combination of references does not teach a path including a different plurality of a plurality of nodes where a time out value is stored in each node in all of the paths and not just in the identified path in combination with setting a time out value by adding a period of time or percentage of the measured latency to the time out value. Therefore, the combination does not render Applicant's claims unpatentable.

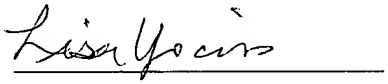
The Examiner also stated that neither *Chang* nor *Cisnerso* teaches that non-optimal timeout values result in the client waiting an excessive time period before recognizing a failure to respond on the part of the server. The Examiner used *Suzuki* to add the features believed missing from the combination of *Chang* and *Cisnerso*.

The combination of references does not teach a path including a different plurality of a plurality of nodes where a time out value is stored in each node in all of the paths and not just in the identified path in combination with non-optimal timeout values resulting in the client waiting an excessive time period before recognizing a failure to respond on the part of the server. Therefore, the combination does not render Applicant's claims unpatentable.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 02.03.05

Respectfully submitted,



Lisa L.B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicant